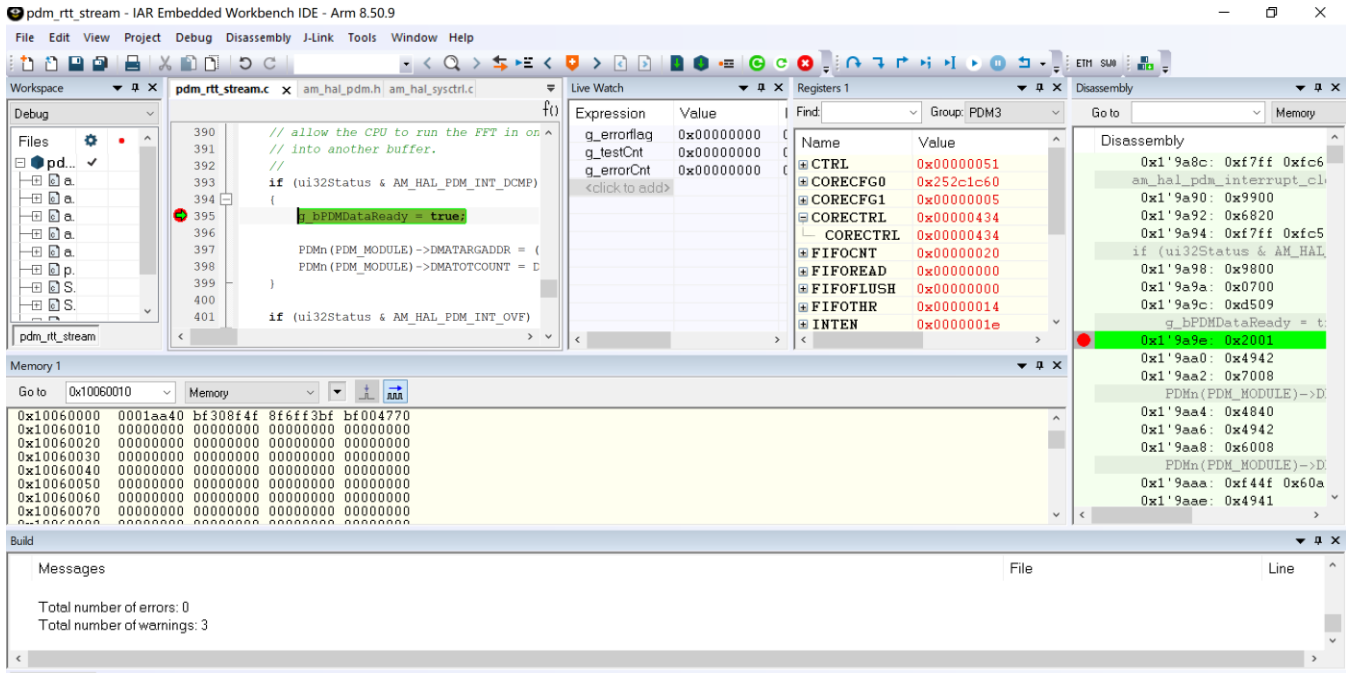
HUAWEI Remote Control Cannot Recognize Voice Instruction Issue Periodic Report

October 2023

Issue Description

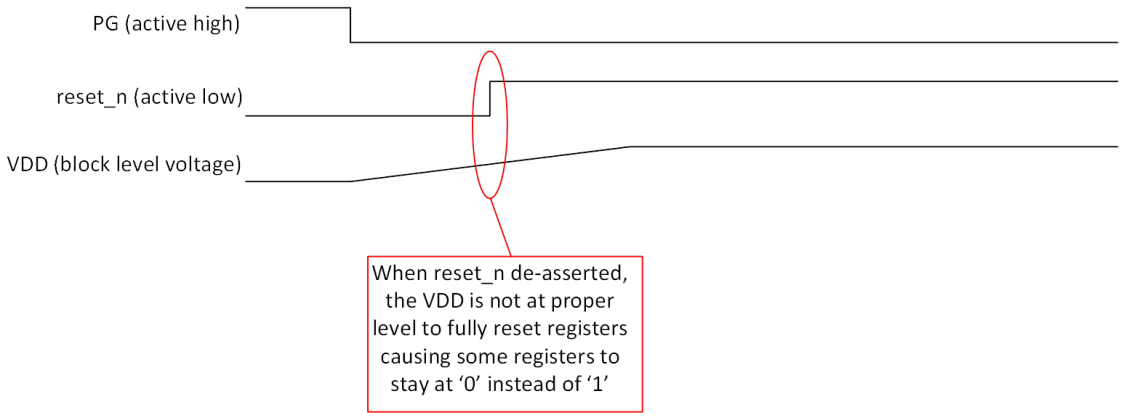
- **Affected Device:**
  - Apollo4 Blue (AMA4B2KK-KBR-B2)
- **Description:**
  - After switching to button mode, some of the controller shows the issue phenomenon that voice instruction cannot be recognized by SmartTV, it may be recovered soon.
  - We use IAR attach to check the PDM DMA buffer once PDM DCMP interrupt comes, and at this time, it shows invalid data with all ‘0’ in the buffer.

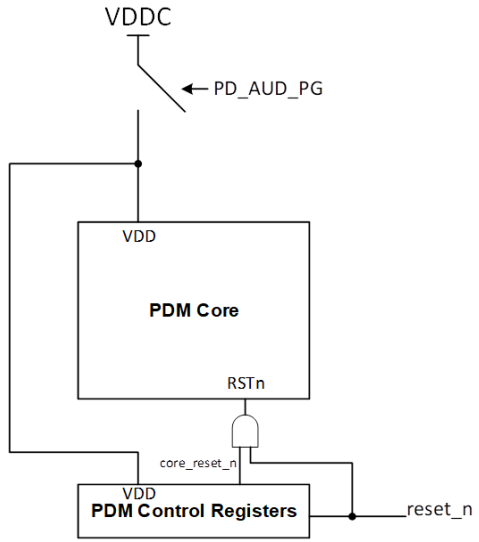


Note:
PDM buffer all ‘0’ when issue reproduced.

Analysis – PDM PG and hresetn Analysis (Root cause)

- PD_AUD_PG 0 means the control to the power switch is turned on
- We have evidence to suggest that the delay to fully ramp the voltage domain of the PDM block after PG de-assertion is longer than the delay from PG to reset_n de-assertion.
- As such, reset could be de-asserted **before the PDM power rail is fully ramped up**, so those FF (Flip-Flop) that **are resetted to high but cannot go high**
- During issue case registers check, all belongs to expect 1 but as 0, which aligns the analysis result here.
- This only affects the configuration registers since, as part of the init sequence, we have a separate reset to the PDM core logic which ensures the core registers are properly initialized. See diagram lower right corner.





Analysis – PDM.CORECTRL[31] is unintentionally cleared

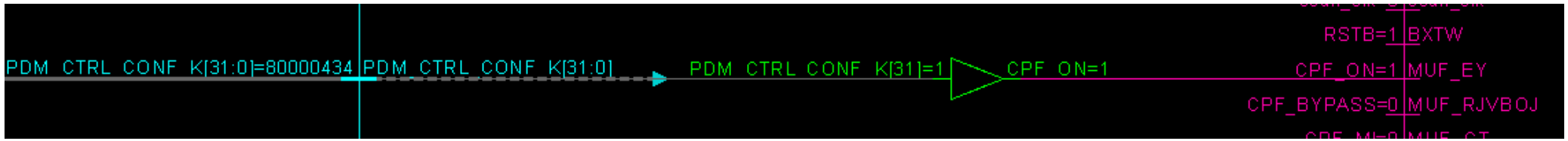
- We have dumped PDM register when it's normal and when produced, find PDM.CORECTRL[31] bit is unintentionally cleared, this led to input data to be all '0'.
- We use AM_CRITICAL_BEGIN/AM_CRITICAL_END to surround PDM_init() function to avoid other thread modify it, and find this bit is cleared at very beginning of the initialization sequence, just after PDM powered on: **am_hal_pdm_power_control(PDMHandle, AM_HAL_PDM_POWER_ON, false);**
- On EVB, we can also see the similar phenomenon if bit31 cleared.

```
296 J-Link>mem32 40204000 100
297 40204000 = 00000051 252C1C60 00000005 80000434
298 40204010 = 00000012 00001018 00000000 00000014
```

```
245 J-Link>mem32 40204000 100
246 40204000 = 00000051 252C1C60 00000005 00000434
247 40204010 = 00000020 00000000 00000000 00000014
```

* PDM.CORECTRL reg(0x4020400C) is unexpectedly cleared

- CORECTRL[31] is the enable signal for internal filter, if it was disabled (0), output data will be zero



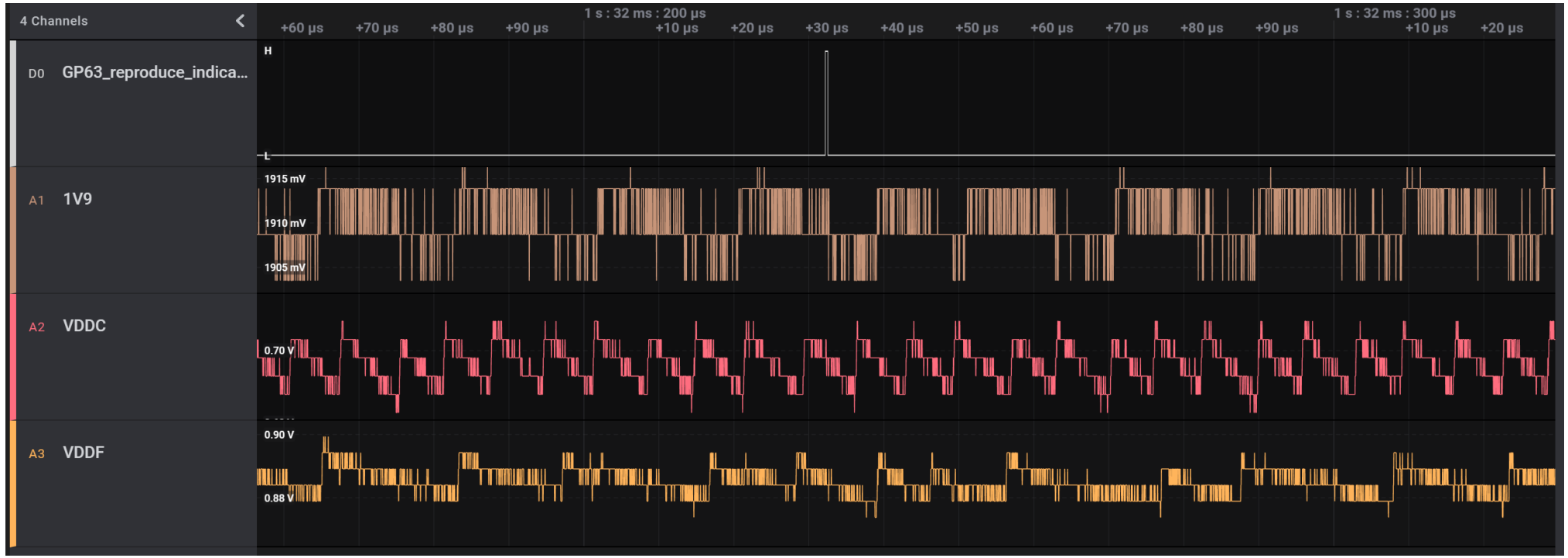
Analysis – Issue phenomenon check

- When the issue happened, we saw other PDM modules also has unexpected power-on reset values
- We saw abnormal values show up with multiple registers
- Same board with multiple reproducing cases, the abnormal value might change
- All abnormal is expected to be 1 but as 0

NO.	Abnormal register/Value	Expected Power-on reset value	Bit phenomenon
#3 (1st dump)	PDM2.CORECFG0 (0x21080**B**64) PDM3.CORECTRL (0x**0**0000**2**4)	0x21080**F**64 0x**8**0000**3**4	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0
#3 (2nd dump)	PDM2.CORECFG0 (0x21080**B**64) PDM3.CORECTRL (0x**0**0000**20**)	0x21080**F**64 0x**8**0000**34**	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0
#3 (3rd dump)	PDM2.CORECFG0 (0x21080**B**64) PDM3.CORECTRL (0x**0**0000**2**4)	0x21080**F**64 0x**8**0000**3**4	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0
#4 (1st dump)	PDM2.CORECFG1 (0x**2**) PDM2.CORECTRL (0x8000043**0**) PDM3.CORECFG0 (0x210**0**0**B**64) PDM3.CORECTRL (0x**0**0000**0**30)	0x**3** 0x8000043**4** 0x210**8**0**F**64 0x**8**0000**4**3**4**	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0 suppose 1 but read 0 suppose 1 but read 0
#4 (2nd dump)	PDM2.CORECFG1 (0x**2**) PDM2.CORECTRL (0x8000043**0**) PDM3.CORECFG0 (0x210**0**0**B**64) PDM3.CORECTRL (0x**0**0000**0**30)	0x**3** 0x8000043**4** 0x210**8**0**F**64 0x**8**0000**4**3**4**	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0 suppose 1 but read 0 suppose 1 but read 0
#4 (3rd dump)	PDM2.CORECFG1 (0x**2**) PDM2.CORECTRL (0x8000043**0**) PDM3.CORECFG0 (0x210**0**0**B**60) PDM3.CORECTRL (0x**0**0000**0**30)	0x**3** 0x8000043**4** 0x210**8**0**F**64 0x**8**0000**4**3**4**	suppose 1 but read 0 (i.e. 1->0) suppose 1 but read 0 suppose 1 but read 0 suppose 1 but read 0

Analysis – HW environment check

- We measured the power rail (1V9/VDDC/VDDF) when issue occurred, GPIO63 is used to indicate when the issue reproduced.
- Seems nothing abnormal here.



- If HFADJ/HFADJ2 disabled, bit31 is also cleared when issue occurred.

Software Solution

- After PDM power on, in the case of a non-default register value, write the registers to their default value.
- We already verified it on the multiple known issue boards (#1, #3, and #4), all without issue anymore.
- This change will be included in Ambiq's later SDK release.
- Patch file already provided to Huawei software for integration.

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endpoint intelligence

Thank you