QUICK START GUIDE

Apollo4 EVB

(EVB Revision 3)

Ultra-low Power Apollo SoC Family

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1. Introduction

This document provides guidance in setting up the Apollo4 Evaluation Board (EVB), revision 3, part number AMAP4EVB, to get started executing code examples, measuring power consumption in various configurations, and beginning software development.

This version of the EVB contains silicon version B2 of the Apollo4 SoC.

2. Document Revision History

Rev #	Date	Description
3.0	Jul 2021	Initial release for EVB revision 3
4.0	Aug 2021	Updates: - Reference Documents and Software section added - Quick Start section added - Parts Location drawings added - Ordering Information section added

Table 1: Document Revision History

3. Reference Documents and Software

The following items may be useful in understanding and using the EVB.

- EVB Schematic
- Apollo4 SoC Datasheet
- Apollo4 Programmer's Guide
- Apollo4 Errata List
- AmbiqSuite SDK

4. Quick Start

The EVB Kit comes with the following items:

- Apollo4 Evaluation Board (EVB), revision 3
- USB Type C cable
- Four adhesive-backed rubber feet
- Extra jumpers

Caution: The EVB has components loaded on the back of the board. Care should be taken to not damage these components. The included rubber feet should be applied to the bottom of the board to prevent direct contact between the components and a desk surface.

The EVB comes with jumpers pre-configured for default operation. Also, it has been pre-programmed with the Binary Counter example program. To start EVB program execution, connect the USB-C cable from a USB port on a PC to the J-Link USB connector (J6) on the EVB, and turn on the power switch (SW4). The blue LED under the power switch should illuminate.

Monitor the three LEDs on the bottom of the EVB (D3-D5). The LEDs should light in a binary count-up pattern, and repeat.

The AmbiqSuite SDK provides many example programs that may be run on the EVB. To run these examples, download the SDK via the link provided above and select any of the pre-built examples in the SDK at /boards/apollo4b_bga_evb/examples.

5. Overview of the Apollo4 EVB

The Apollo4 EVB, version 3, features Arduino-compatible headers and an integrated J-Link debugger:

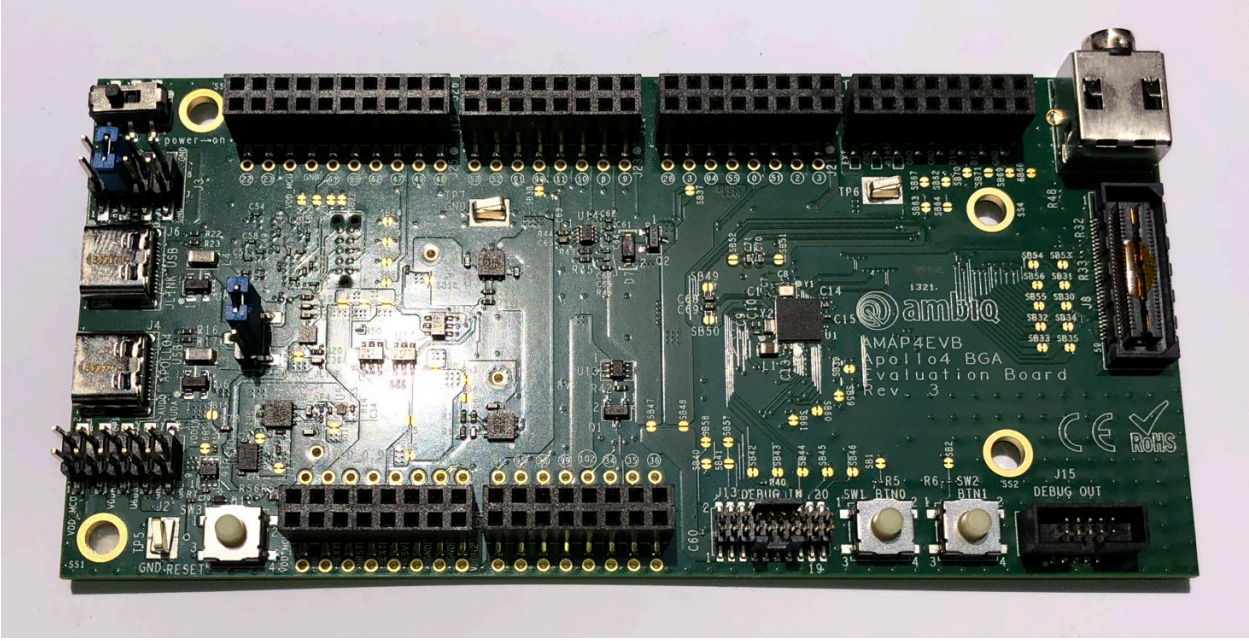

Figure 1. Apollo4 EVB Revision 3

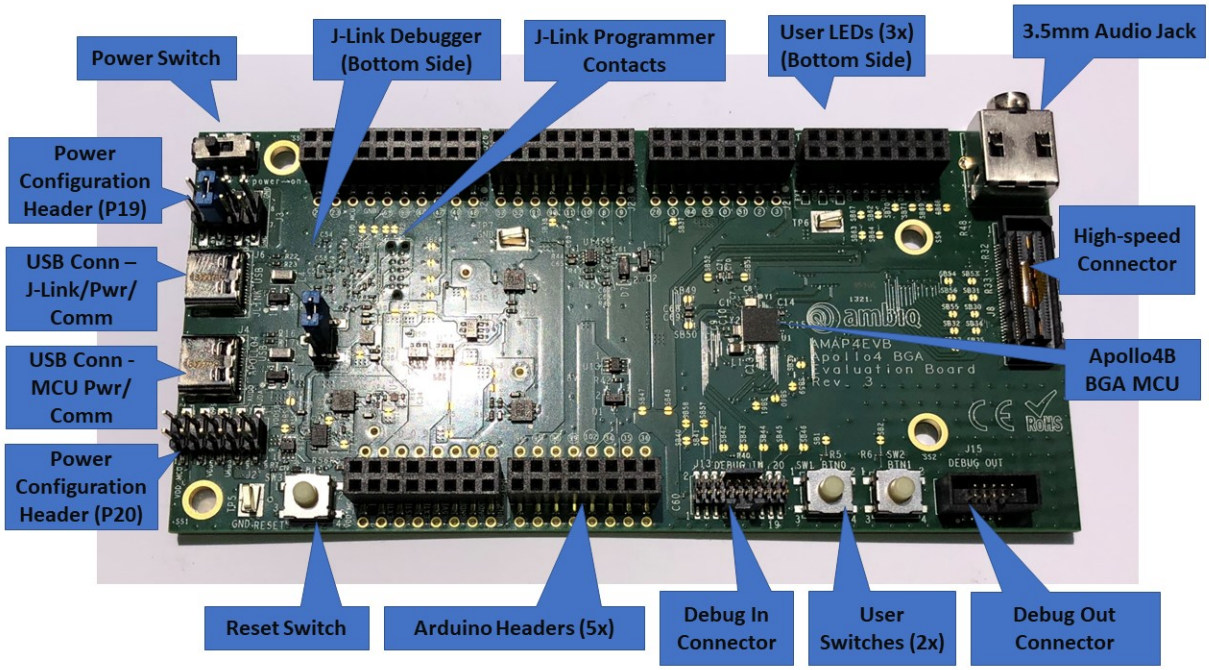

Figure 2. Apollo4 EVB - Major Components

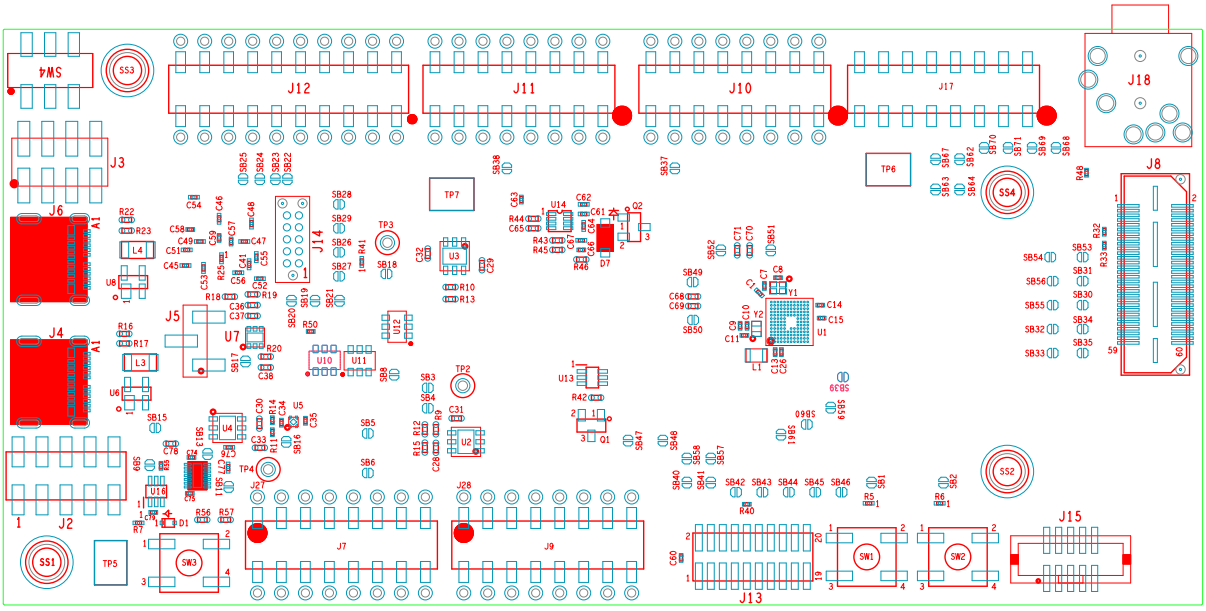

Figure 3. Apollo4 EVB - Top-side Parts Location

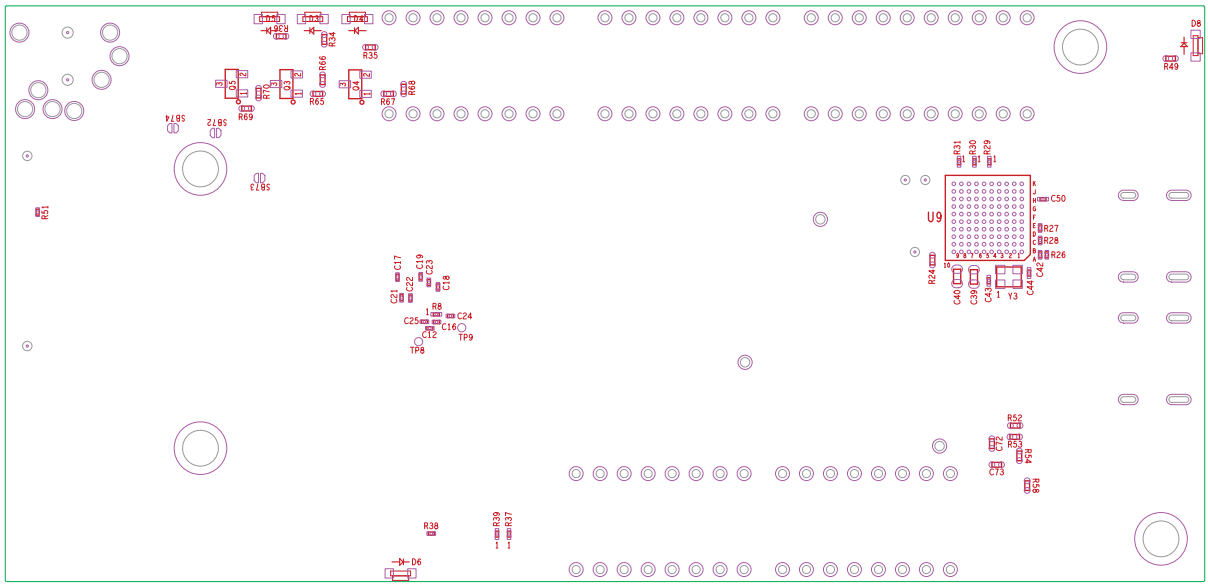

Figure 4. Apollo4 EVB - Bottom-side Parts Location

The EVB has these features:

- Apollo4 SoC in the BGA package (AMAP42KK-KCR-B2)
- Low power reference design
- Multiple power/clock options
- USB Type C connector for power/download/debug

- USB Type C connector for power/data to Apollo4
- Segger J-Link debugger
- Debugger-in port (J13) (SWD or ETM)
- Debugger-out port with connection-indication LED (J15)
- Three user-controlled LEDs
- Two push buttons for application use, plus a reset push button
- Power slide switch with LED power indicator
- Five Arduino-style headers (J7, J9-J12) for pin/power access to a shield board
- Test points for power measurements
- High-speed connector (J8 - QSH-030-01-L-D-A) for interfacing to displays and/or high-speed memory
- Multiple solder-bridge options for power supply flexibility and peripheral access options
- 3.5 mm audio jack (SJ-435107) for evaluating low-power analog audio interface
- CE Mark and RoHS compliant

5.1 Secure Boot on the Apollo4 SoC

Apollo4 SoC parts from the Ambiq Micro factory are preprogrammed with a Secure Bootloader and an uninitialized Customer Info Space, referred to as INFO0. Initial provisioning of the part would include programming a valid INFO0 and programming the main firmware image in the flash. The Apollo4 EVB is shipped with the INFO0 configuration pre-programmed with optimal settings for the EVB layout:

1. Default boot to non-secure mode
2. Enable Boot Override to Push Button on GPIO18 (OTP setting) - BTN0/SW1
3. Enable wired updates over UART0
    A. UART0 is mapped to JLINK (OTP Setting).
    B. Baud rate is 115200 bps, no-parity, 8-bit data length, no flow control.
    C. Timeout is 3 seconds.

For your reference, the following settings are programmed into INFO0 on the Apollo4 SoC resident on the EVB:

- Simo Buck is NOT enabled.
- Secure Bootloader (SBL) interface is configured to UART using GPIO47 and GPIO60, which allows secure boot to be performed over the J-Link COM interface of the EVB.
- SBL override pin is configured to GPIO18 which is BTN0/SW1 on the EVB.
- All Flash and Debugger protection features are disabled.

For information on changing the INFO0 settings as well as using the Secure Bootloader, please refer to the *README.txt file*, which can be found in the tools\apollo4b_scripts folder of the latest SDK release supporting the Apollo4 family. This folder contains a number of python scripts to demonstrate generation of INFO0 settings, customer main images, and the creation of images for the Wired Update protocol over UART.

6. Debug Interface

Figure 5 shows the Apollo4 EVB set up for standard debug using the on-board J-Link debugger and on-board power supply. The on-board J-Link debugger is on the other side of the board and not shown in the figure.

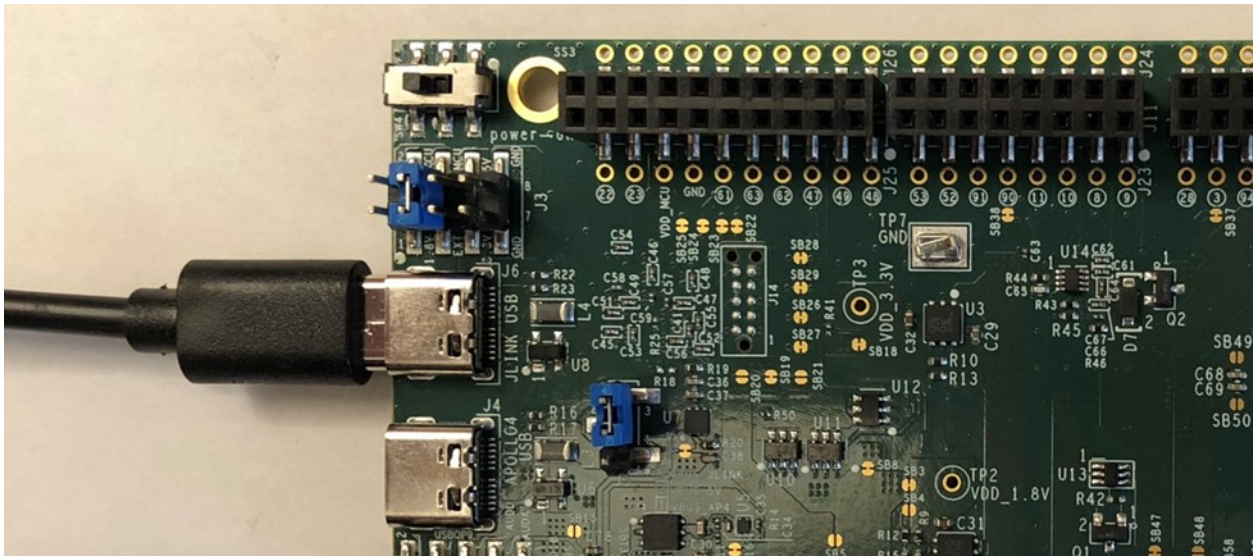

Figure 5. Apollo4 EVB Using On-board J-Link Debugger

The debug interface is supported by standard J-Link drivers from Segger. Please refer to “Software Development Tools” on page 16 for more details on J-Link debug support.

6.1 Use of External Debugger

This EVB also supports the use of an external Cortex SWD debug interface through a 20-pin debug header (DEBUG IN - J13) as shown in Figure 6. See the EVB schematic for connector pinout.

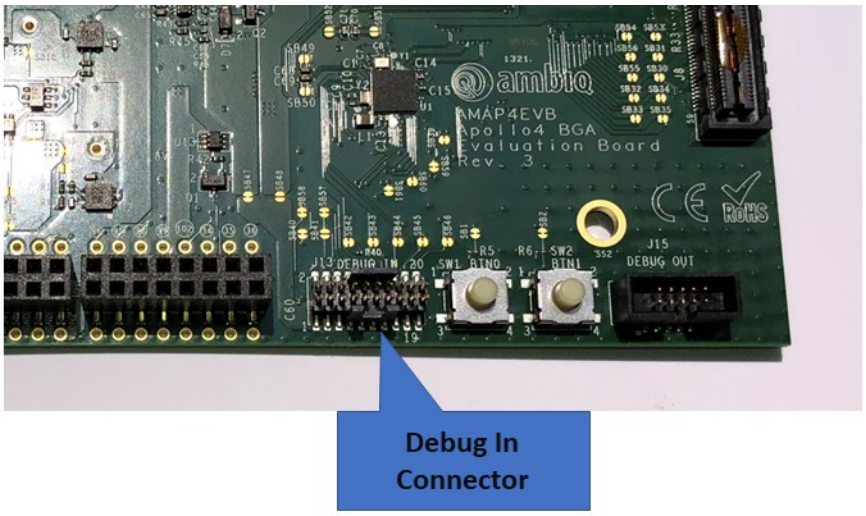

Figure 6. Apollo4 EVB's DEBUG IN Header (J13)

No jumper changes are required to use an external debug adapter. Simply connect the external debug adapter with a 10-pin ribbon cable connector to the "DEBUG IN" header.

6.2 Use of J-Link Adapter as an External Target Board Debugger

The EVB also offers the ability to be used as a J-Link debug adapter for any target board that has an Apollo family MCU.

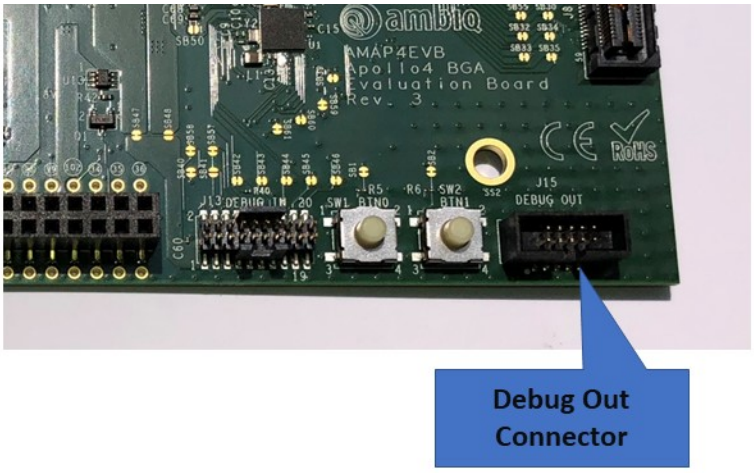

Figure 7. Apollo4 EVB's DEBUG OUT Header (J15)

To utilize this functionality, use a 10-pin low-pitch standard debug connector to connect the "DEBUG OUT" header (J15) on the EVB to the debug header on the target board. The EVB will automatically detect when the "DEBUG OUT" header is connected to another target board and reconfigure the integrated J-Link to connect to this external board rather than the on-board Apollo4. See the EVB schematic for connector pinout.

Note: A voltage on pin 1 of the J15 header is required for the above mentioned automatic switch to occur. Also, if the target VDD doesn't match the on-board VDD_1.8V voltage (1.9V default), and to avoid possible voltage level conflicts on the debug I/O port, VDDIO of the J-Link processor should be changed to the target voltage by cutting SB19 and shorting SB20 (VDD_EXT) or SB21 (VDD_EXT_DBG). See “Power Supply Options and Measuring Current” on page 17.

7. Software Development Tools

The standard Segger J-Link debug interface is used on the Apollo4 EVB. Please install the latest Segger J-Link software, and configure your preferred development IDE (Keil, IAR, or Eclipse) to use J-Link debug interface.

Links to development tools that support Apollo4:

- SEGGER J-Link Software (6.96 or later): https://www.segger.com/downloads/jlink
- KEIL uVision 5 (MDK5.34 or later): https://www.keil.com/demo/eval/arm.htm
- Latest Keil Pack (Also used by Eclipse): http://www.keil.com/dd2/pack/#/third-party-download-dialog
- IAR Version (8.42.2 or later): https://www.iar.com/iar-embedded-workbench/tools-for-arm/arm-cortex-m-edition/
- GCC 5.3.1: https://gcc.gnu.org

Regardless of preferred IDE, please install the Segger J-Link software. All of the above development environments support J-Link, but you must have the latest J-Link software installed. Most alternate development environments also are supported by J-Link.

Please refer to the AmbiqSuite Getting Started Guide (AMSDKGS) provided with any SDK release for more details on setting up development IDEs to use J-Link.

8. Power Supply Options and Measuring Current

The Apollo4 EVB is intended to operate off of a 5V supply, which is used to generate downstream voltages.

There are two power supply options for the Apollo4 EVB SoC:

- Operate at 1.9V by default as provided by the on-board power supply (referred to as nominal "VDD_1.8V"). This can be adjusted to 1.8V by shorting SB4 shown on the Power Supplies page of the EVB schematic(1).
- Provide externally supplied power.

The Apollo4 EVB utilizes solder-bridges for connecting and disconnecting rails from power supplies, whether generated on-board or off-board. Figure 8 shows the solder-bridge connection strategy between various on-board power supplies and Apollo4 power rails.

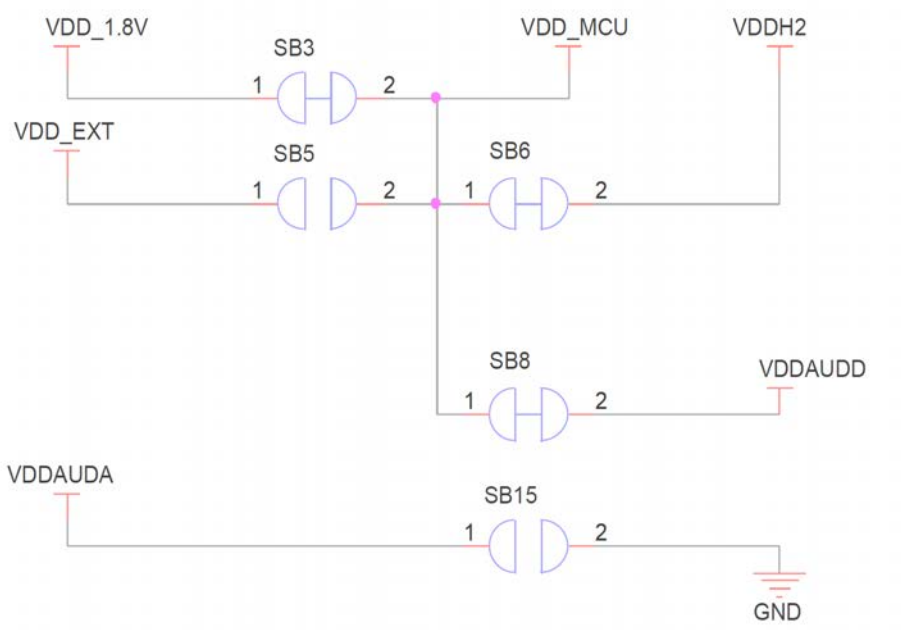

Figure 8. Apollo4 EVB Power Supplies Solder Bridge Connection

Figure 9 shows the USB power sequencing circuit producing the voltage supplied to VDDUSB33 and VDDUSB0_9 through solder-bridges SB13 and SB11, respectively. These solder bridges are shorted by default.

1. Refer to the EVB schematic and assembly drawing for purpose and location of all solder bridges on the EVB.

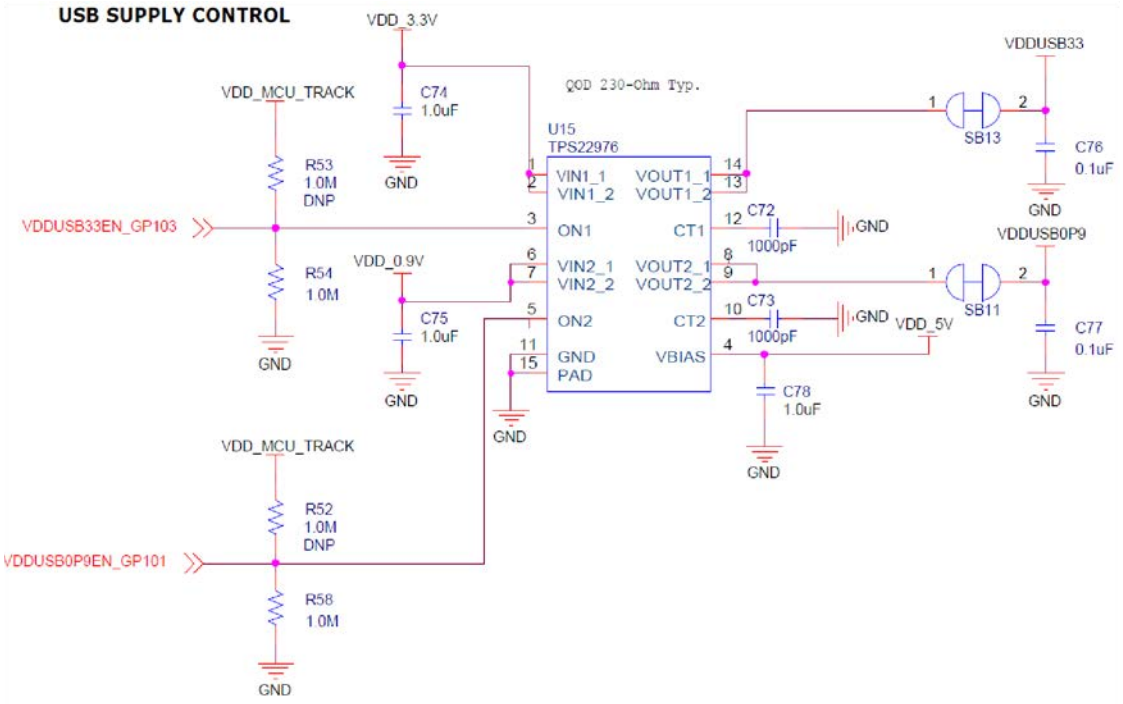

Figure 9. Apollo4 EVB USB Power Sequencing Circuit

Similarly, Figure 10 shows the power sequencing circuit producing the voltage supplied to the MIPI VDD18 supply through solder-bridge SB9. This solder bridge is also shorted by default.

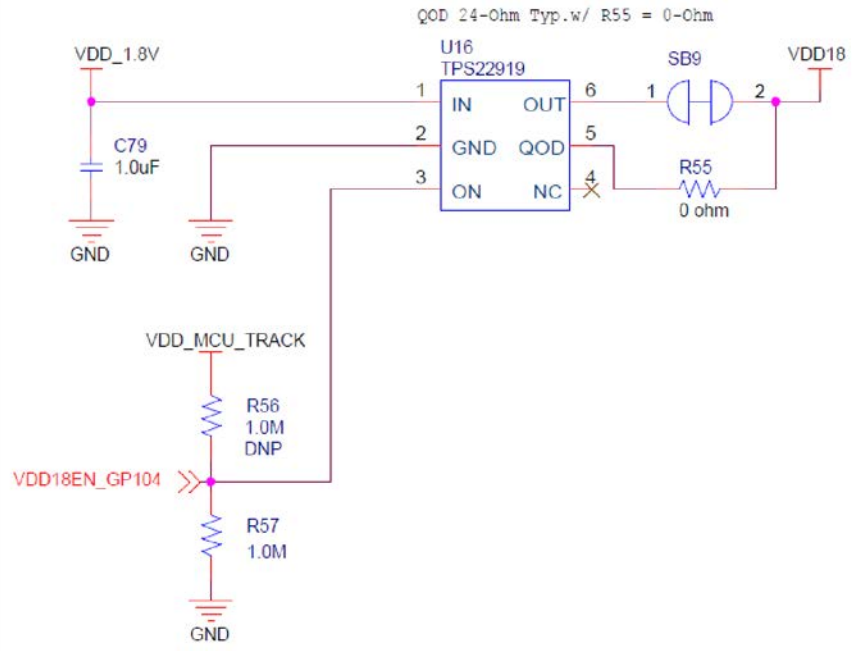

Figure 10. Apollo4 EVB VDD18/MIPI Power Sequencing Circuit

As shown in Figure 11 and Figure 12, headers J2 and J3 provide easy access to the various system and chip-level power supplies present on the EVB. These can be used in conjunction with the above solder-bridges to measure current, monitor voltage, or provide externally generated power to each specific rail.

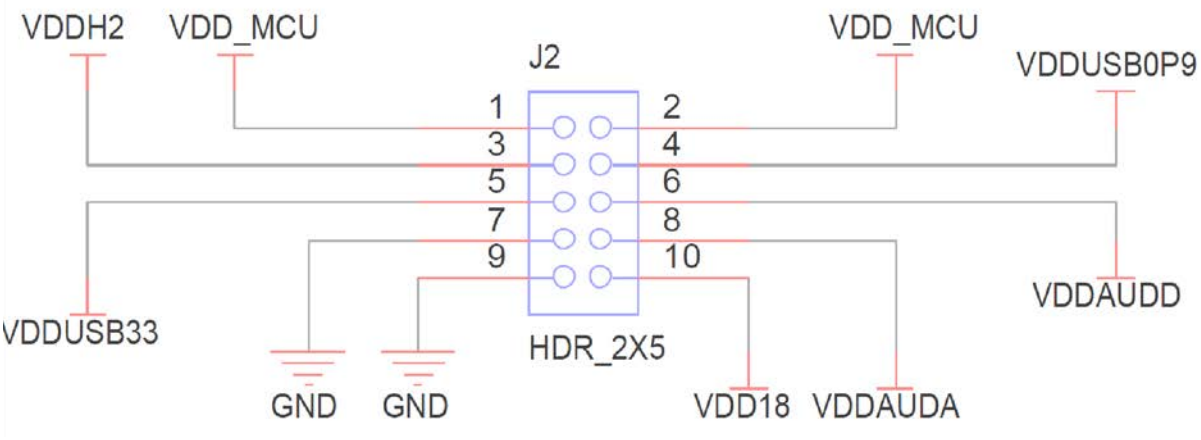

Figure 11. Apollo4 EVB Voltage Selection on Header J2

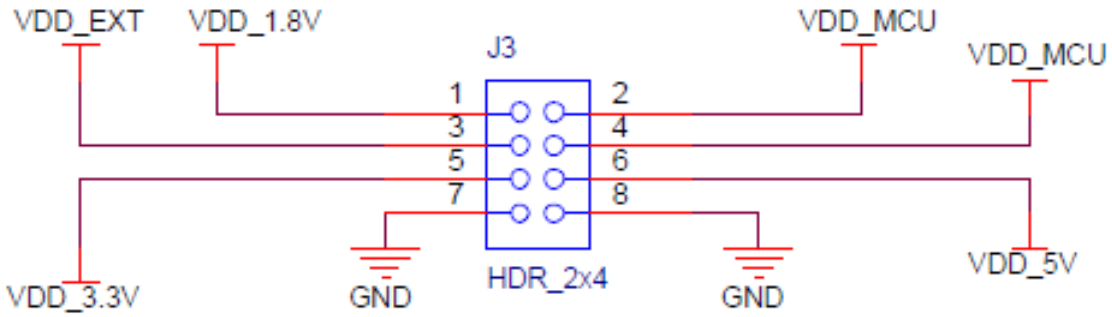

Figure 12. Apollo4 EVB Voltage Selection on Header J3

If the user would like to use a separate power supply for the EVB, then SB3 shown in Figure 8 should be cut, and either SB5 should be shorted with solder or pins 3 and 4 of J3 should be jumpered). The external power rail can be applied to VDD_EXT on J3, pin 3. Consult the electrical specifications in the Apollo4 Datasheet for the acceptable operating range for VDD_MCU.

Note that the JLINK I/O voltage should be set to the new VDD_IO of the chip, and therefore SB19 (not shown in Figure 8) should be opened and SB20 should be shorted (soldered).

Note also that the use of the on-board SoC supply may be restored by disconnecting the external supply and either shorting SB3 once again or by jumpering between pins 1 and 2 of J3. The J-Link I/O voltage also should be restored.

9. Non-Power Solder Bridges

9.1 Solder Bridges for Reducing Trace Length to Optimize Performance

The following peripherals support solder-bridge connections, which allow for optimized performance by reducing overall trace length at the cost of losing connectivity to their respective GPIO headers. Note that these connections can be reset by applying solder across the solder-bridge.

Peripheral	GPIO	Description
Display Controller, MSPI0	37, 64-73	Opening solder-bridges connects these GPIO exclusively to J8, with minimal trace stubs
ETM	50-54, 55 (open by default)	Opening solder-bridges connect these GPIO exclusively to J13. SWO is default connection to J13 (shared with GP55, SWTRCTL)

Table 2: Peripherals Supporting Solder Bridge Connections

Additionally, the LED indicators can be disconnected from GPIO30, GPIO60 and GPIO90 by opening their respective solder-bridges (SB37, SB39, and SB38). GPIO47, GPIO58, GPIO59 and GPIO60 are used for UART communication with the on-board J-Link. Opening SB26-SB29 frees these pins for exclusive use with the standard GPIO headers J10 and J12.

9.2 Solder Bridges for Audio Selectivity

As shown in Figure 13, a single audio jack, J18, provides stereo audio input routed to AUDADC (also referred to as LPADC) inputs on the SoC. Alternatively, up to 4 single-ended or 2 differential pair audio signals as shown in Figure 14 can be input on connector J17 which is routed on the EVB as differential pair(s) to AUDADC inputs. The default (shorted) solder bridge configuration enables either of these input options.

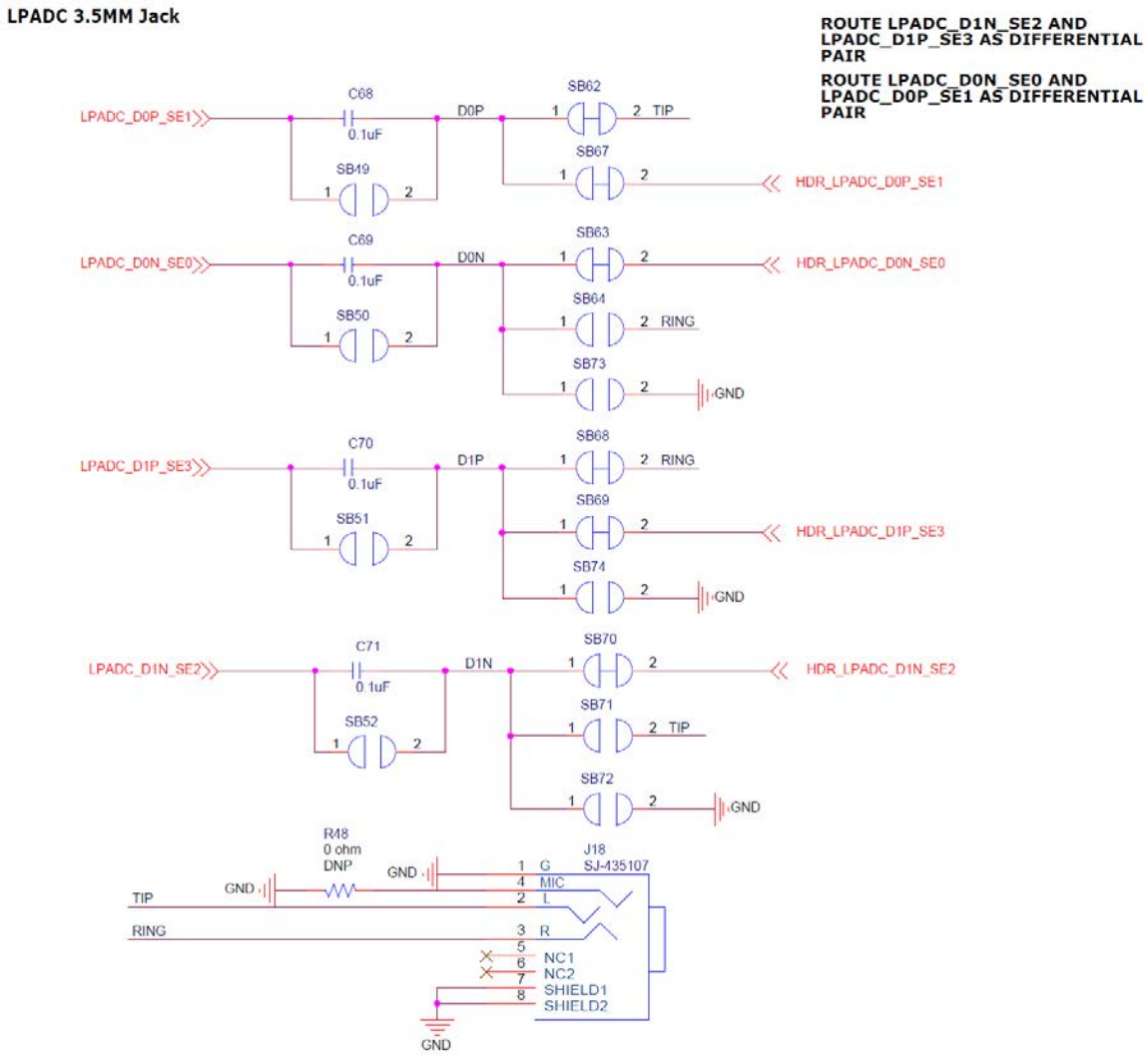

Figure 13. Audio Jack J18 and AUDADC Audio Source Selections

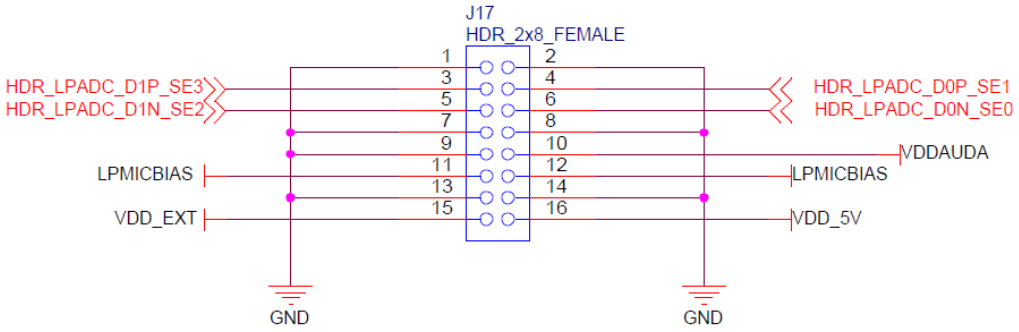

Figure 14. Audio Header J17

10. Ordering Information

Table 3: EVB Ordering Information

Device Name	Orderable Part Number	EVB Revision	SoC	SoC Package	Temperature Range	Availability
Apollo4 EVB	AMAP4EVB	3	Apollo4	146-pin BGA	–40 to 85°C	Now

Table 4: SoC Ordering Information

Device Name	Orderable Part Number[a]	MRAM	RAM	Package	Packing	Temperature Range	Availability
Apollo4 SoC	AMAP42KK-KCR-B2	2 MB	1.8 MB	146-pin BGA	Tape and Reel	–40 to 85°C	Now

a. The silicon revision is identified by the first letter in the bottom row of the package's top marking: E = revision B1, F = revision B1+, G = revision B2, H = revision B2+.

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