Apollo4 BLE Controller Datasheet

Doc. ID: DS-A4BLE-0p2p0

Revision 0.2.0

April 2020

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1. Document Revision History

Table 1: Document Revision History

Revision	Date	Description
0.1.0	Apr 2020	Document initial release
0.2.0	Apr 2020	General Updates - Introduction: Removed cache from Fig. 1; updated feature set - Clocking: Corrected text about 32 KHz crystal connection - MCU Interface: Several sub-sections moved to Apollo4 Programmer's Guide - Electricals - Updated receiver sensitivity and SPI clock frequency specs

2. Introduction

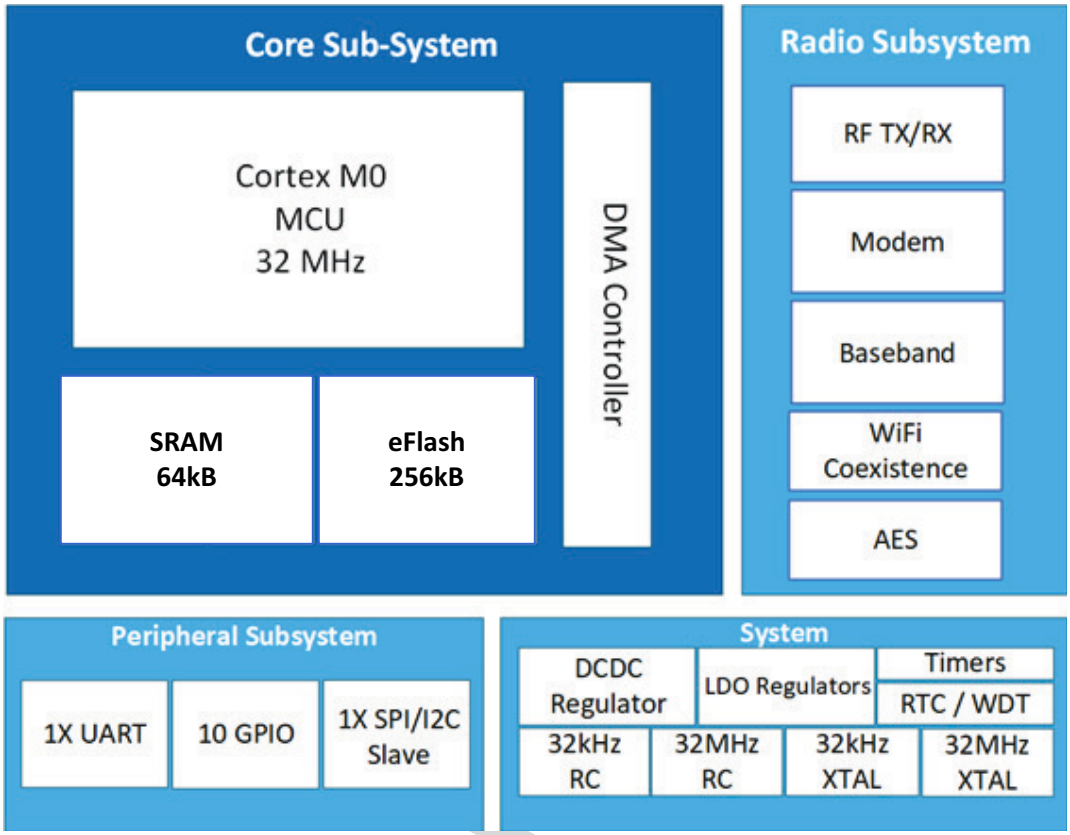

Figure 1. Apollo4 BLE Controller Block Diagram

The block diagram of the Apollo4 BLE Controller is as shown in Figure 1. The controller is designed to efficiently interface as a companion device to the Apollo4 MCU and provide low power BLE 5.1 connectivity. The Apollo4 BLE Controller incorporates a dedicated ARM Cortex-M0 processor, baseband, modem, RF and corresponding PMU, clocking, I/O and memory. BLE includes 256 KB non-volatile memory for code store.

The BLE Controller interfaces through a Host Controller Interface (HCI) and an efficient SPI physical interface. The Link Layer (LL) and Physical Layer (PHY) of the controller stack execute within the M0 BLE Controller, offloading control of these two layers from the host Apollo4 MCU.

3. Feature Set

Energy efficient ARM Cortex-M0 MCU

- 256 KB Flash including link layer stack
- 64 KB SRAM
- 32 MHz MCU and Flash speed
- I2C and SPI slave
- UART, timers, WDT

Bluetooth 5.1 Low Energy Technology

- Full feature set BLE 5.1 Controller Subsystem
- High Data Rate (2 Mbps)
- Advertising extensions
- WiFi coexistence
- Angle of Arrival/Departure Support
- Up to 10 simultaneous links supported
- AES-128 hardware acceleration

Integrated Power Management

- 1.71 - 3.63 V Support
- DCDC Regulation
- Retention LDO for low power sleep mode

Low Current Consumption

- 3 mA typical peak receiver current
- 3 mA typical peak transmitter current at 0dBm
- 1.5 uW sleep mode (all memory in retention)

High Performance RF

- -96 dBm BLE RX sensitivity @ 1 Mbps
- -93 dBm BLE RX sensitivity @ 2 Mbps
- -20 to +6 dBm (0.5 dBm steps) transmitter output power

4. Functional Overview

The Apollo4 BLE Controller, shown in Figure 1, is a companion solution for Apollo4 MCU. The Apollo4 BLE includes an ARM Cortex-M0, BLE baseband, modem and 2.4 GHz transceiver. Communication with the BLE Controller is supported through a high speed SPI interface. Dedicated data movement hardware enables efficient interface for HCI packet transfers.

The Apollo4 BLE can operate internally at different clock frequencies as required for the communication workload. The supported clock input frequency is 32 MHz. The BLE incorporates a PLL to generate the necessary clocking for the BLE subsystem. The reference clock for the PLL can be sourced from either a dedicated external crystal or a single-ended clock input from the Apollo4 MCU. Power regulation is supported internally via a buck DCDC regulator and supporting LDO regulators needed to generate all internal voltages for the radio and digital subsystems.

5. Clocking

The Apollo4 BLE Controller supports Crystal clock and single-ended clock sources. In the case where the BLE Controller is stand-alone or configured to have its own clock source, a 32 MHz and/or 32 KHz crystal is required. The 32 MHz crystal is connected to the XO32M pins as shown below. The 32 KHz crystal is connected to the XO32 pins as shown below. The clocking configuration must be set in the CLKCONFIG register accordingly. At reset, the internal RC oscillators are enabled. The host MCU must change the clock configuration in CLKCONFIG and also set the appropriate mux settings in the GPIOCONFIG register.

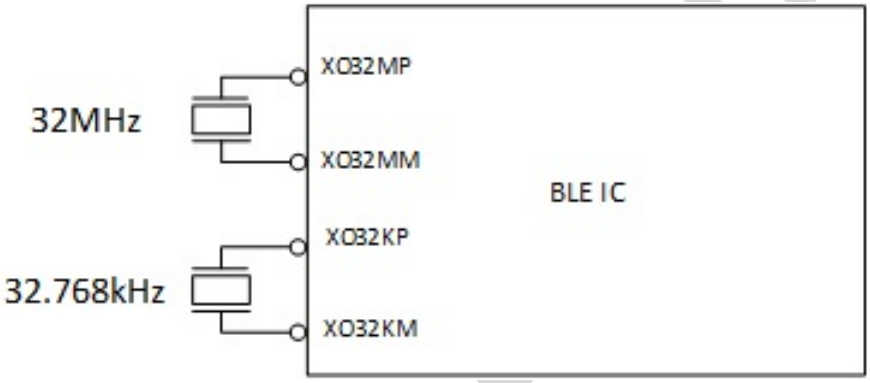

Figure 2. Crystal Configuration

When coupled with the Apollo4 MCU, the clocks can be sourced only when required from the MCU to the BLE Controller. In this configuration, the 32 MHz clock is driven on XO32MP as a single-ended signal. The 32 KHz clock is driven on XO32kP as a single-ended signal. The CLKREQ (GPIO) and CLKACK (GPIO) signals are used to drive clock request and acknowledge to the MCU. This allows the MCU to power down the high frequency crystal to save power. The low frequency clock is always running when interfaced with the BLE Controller.

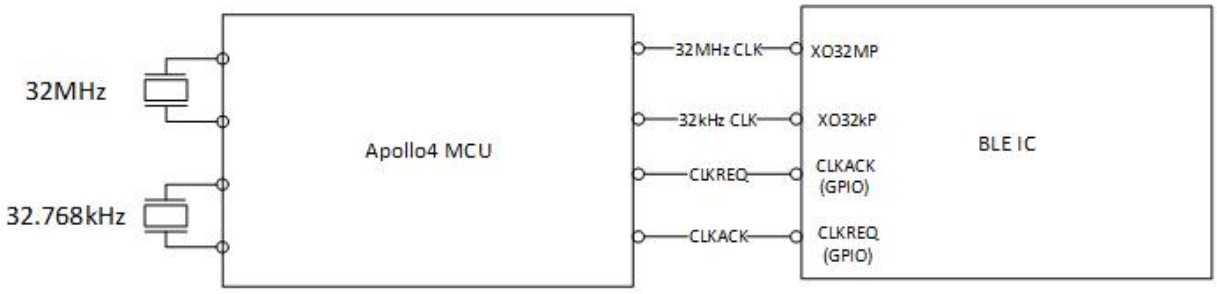

Figure 3. MCU Clock Source Configuration

The BLE Controller has an integrated PLL for generating the high frequency clocking required for the 2.4 GHz radio.

Below illustrates the handshake for the high frequency clock.

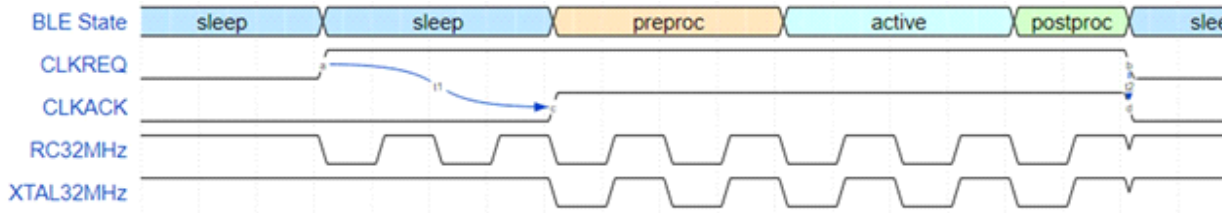

Figure 4. High Frequency Clock Handshaking

- On wake event, BLE controller utilizes internal RC and asserts CLKREQ (transition ‘a’)
- Apollo4 MCU initiates XTAL startup and asserts CLKACK once stable (transition ‘c’)
  - ‘t1’ delay is targeted for <500 us
- XTAL32MHz is stable and available at or before CLKACK assertion
  - XTAL32MHz will be gated ‘high’ when disabled
- BLE controller should stay in deepest power state possible until CLKACK is asserted
- On “sleep” event, BLE controller deasserts CLKREQ (transition ‘b’)
- Apollo4 MCU gates
- XTAL32MHz and optionally powers down XTAL
- Apollo4 MCU deasserts CLKACK (transition ‘d’)
  - XTAL32MHz is gated ‘high’ when disabled
  - ‘t2’ delay should be within 1-2 32 MHz clocks

6. Power Management

The BLE IC has an integrated DCDC switch regulator as well as LDOs to provide all of the voltage rails for the BLE functionality. There are the following power modes:

- Active
- Idle
- Standby
- Sleep
- Shutdown

The following table describes which functional domains are active, retained or off for each power mode.

Table 2: Domain States

Domain	Power Mode				
	Active	**Idle**	**Standby**	**Sleep**	**Shutdown**
CPU Core	Active	Halt	Off	Off	Off
SRAM	Active / Standby	Standby	Retention	Partial Retention	Off
RF	Active / Standby	Off	Off	Off	
Clock	Active	Active	Active	Gated / Off	Off
Peripherals	Active	Active	Off	Off	Off
Timers	Active	Active	Active	Active	Off

7. MCU Interface

The host MCU (Apollo4) interfaces to the BLE IC via a SPI connection. There are additional sideband signals used to enable clock and power management handshaking.

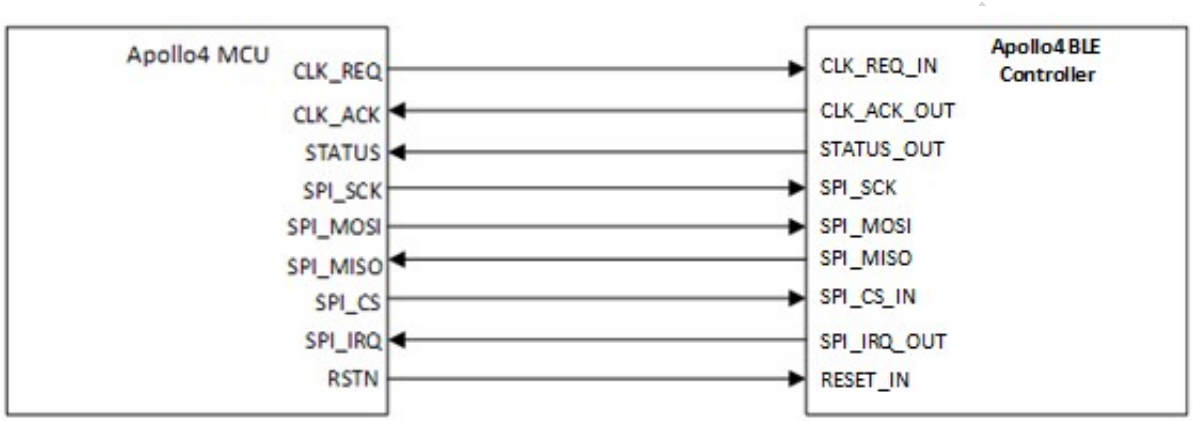

Figure 5. MCU BLE Interface

Table 3: Apollo4 Signal Descriptions

Signal	Description
SPI_SCK	SPI Clock
SPI_MOSI	SPI MOSI
SPI_MISO	SPI MISO
SPI_CS	SPI Chip Select
SPI_IRQ	SPI Interrupt
STATUS	Status indicator
RSTN	Reset signal
CLKREQ	Clock Request
CLKACK	Clock Acknowledge

The clock handshake is described in the Clocking section.

The supported SPI interface frequency is 16 MHz. An assertion of the SPI chip select (SPI_CS) indicates an active transaction initiated by the host. In the case where the BLE IC is in SLEEP mode, the SPI_CS assertion should serve as a wake. The SPI slave controller must always be able to accept a transaction from the host whenever SPI_CS is asserted. The controller must also be able to queue up transactions intended to the host concurrent with transactions from the host. The slave controller uses the SPI_IRQ signal to notify the host of attention.

The STATUS signal is used to indicate the state of the BLE controller. STATUS is de-asserted when the BLE IC is in SLEEP or SHUTDOWN mode and asserted otherwise.

8. Integration Reference

8.1 Power Delivery

The integration diagram in Figure 6 gives a reference implementation for a buck enabled configuration.

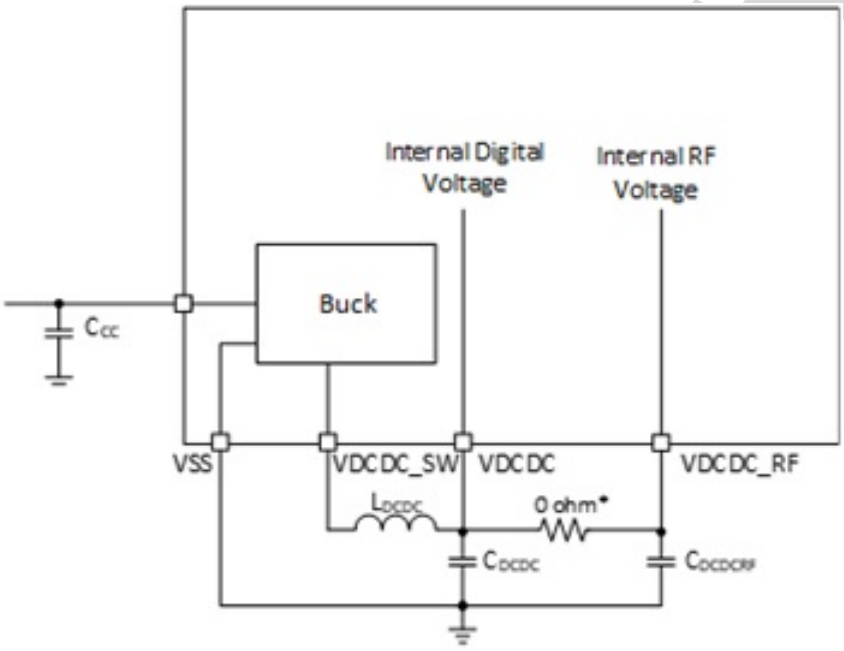

Figure 6. Integration Diagram for Buck Enabled Configuration

8.2 Antenna

The antenna filter shown in Figure 7 is recommended for the Apollo4 BLE Controller.

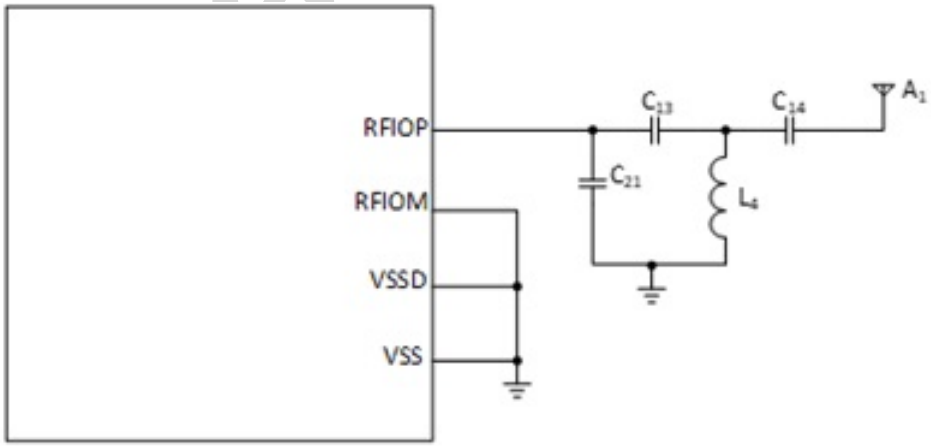

Figure 7. Recommended Antenna Filter

9. Electrical Characteristics

IMPORTANT NOTICE

Specifications and other information in this advanced version of the Apollo4 BLE Controller Datasheet should be regarded as preliminary and subject to change.

9.1 Absolute Maximum Ratings

The absolute maximum ratings are the limits to which the device can be subjected without permanently damaging the device and are stress ratings only. Device reliability may be adversely affected by exposure to absolute-maximum ratings for extended periods. Functional operation of the device at the absolute maximum ratings or any other conditions beyond the recommended operating conditions is not implied.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{DD}	Supply Voltage	VCC pin	1.71	3.63	V
$P_{IN\_MAX\_RF}$	Maximum RF input power	RFIO pin		+10	dBm
T_J	Junction temperature		-40	85	C

9.2 BLE Operating Characteristics and Clocking Specifications

Table 5: BLE Operating Characteristics and Clocking Specifications

Symbol	Parameter[a]	Test Conditions	Min	Typ	Max	Unit
AC Characteristics - Rx						
R_{SENS}	Receiver sensitivity	1 Mbps BLE ideal transmitter, <=37 bytes, PER < 30.8%			-96	dBm
		2 Mbps BLE ideal transmitter, <=37 bytes, PER < 30.8%			-93	dBm
$R_{SENS, VAR}$	Rx sensitivity variance between channels		-0.5		0.5	dB
$R_{RX, MAX}$	Maximum receiver input power	PER < 30.8%			0	dBm
$C/I_{co\text{-}channel}$	Co-channel interference	Wanted signal at -67dBm, modulated interferer in channel, PER < 30.8%		7		dB
PB[b]	Out of band blocking	30 MHz to 2000 MHz		-30		dBm
	Out of band blocking	2003 MHz to 2399 MHz		-35		dBm
	Out of band blocking	2484 MHz to 2997 MHz		-35		dBm
	Out of band blocking	3000 MHz to 12.75 GHz		-30		dBm
F_{ET}	Frequency error tolerance		-125		125	kHz
AC Characteristics – Tx						
P_{OUT_AVG}	Average Tx burst power[c]	Max setting		+6		dBm
$P_{OUT,VAR}$	Average Tx output power variance between channels	TBD	-1		1	dBm
P_{OUT_STEP}	Average Tx output power			0.5		dBm
P_{OUT_HD2}	Second harmonic output power level			-40	-30	dBm

Table 5: BLE Operating Characteristics and Clocking Specifications

Symbol	Parameter[a]	Test Conditions	Min	Typ	Max	Unit
P_{OUT_HD3}	Third harmonic output power level			-40	-30	dBm
P_{OUT_HD4}	Fourth harmonic output power level			-40	-30	dBm
RF						
RF_{IMP}	RFIO Impedance			50		Ω
32MHz Crystal Oscillator						
F_{XTAL}	Crystal frequency			32		MHz
ΔF_{XTAL}	Frequency tolerance	Untrimmed	-40		40	ppm
C_L	Crystal load capacitance			6		pF
ESR	Equivalent serial resistance				100	Ω
T_{XTAL}	Startup time			0.5	1	ms
Phase Noise				-135 @ 10kHz -141.7 @ 100kHz -146.6 @ 1MHz		dBc/ Hz
SPI						
F_{SCK}	SPI Clock Frequency				16	MHz

a. FCC and BQB test reports are available upon request.
b. Modulated RF carrier input signal power level of -67dBm
c. Average Burst Power is Average Power in dBm for all packets included in the demodulation. Power is calculated over 20% to 80% of the duration of each burst.

9.3 BLE Power Requirements

Table 6: BLE Power Requirements

Symbol[a]	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{ACTRX}	Radio Rx Current	Ideal DC-DC		3.0		mA
I_{ACTTX}	Radio Tx Current @ 0dBm	Ideal DC-DC		3.0		mA
I_{SLP}	Sleep mode current	Ideal DC-DC		0.5		µA
I_{SD}	Shutdown mode current	Ideal DC-DC		0.1		µA

a. Measured with Tc= 25C, VCC = 3V and f_{RF}= 2440MHz, unless otherwise noted.

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