

Qualification Testing
1. Reliability Testing Results

Date: 2017/10/15

Product Type: AMA2B1KK-KLR	
Package Type: 4*4 64 LGA Qual Plan #: APOLLO2_LGA_Qual_001 PCN #: N/A	Process Technology: 40nm Fab Location: TSMC, TW Assembly Location: ASE-CL, TW
	Stress Location: ISE Labs, Fremont, CA. USA Test Location: Ambiq Micro, Austin, TX. USA

Test	Conditions	Sample Size/Rejects	Comments
High Temperature Operating Life (Dynamic)	JESD22-A108, +125°C @ 1000 hours, Max Vdd	77/0 77/0 77/0	PASS. QBS to parent devices.
Pre-Conditioning	MSL3 Precon JESD22-A113A, MSL3	160/0 160/0 160/0	Lot1 PASS Lot 2 PASS Lot 3 PASS
Highly Accelerated Stress Test (UHAST)	EIA/JESD22-A118B, +130°C / 85%R.H. Unbiased for 264 hours.	80/0 80/0 80/0	Lot1 @ 264hr PASS Lot2 @ 264hr PASS Lot3 @ 264hr PASS
Temperature Cycle	JESD22-A104, TC condition B(-55C – 125C)	80/0 80/0 80/0	Lot 1 @ 700C PASS Lot2 @ 700C PASS Lot3 @ 700C PASS
ESD HBM: Human Body Model	JESD22-A114F	3/0 3/0 3/0	PASS 2KV. QBS to parent devices.
ESD CDM: Charged Device Model	JEDEC 22-101	3/0 3/0 3/0	PASS 400V. QBS to parent devices.
Latch-up	EIA/JESD78A, 25°C and 85°C, V _{max} = 4.1V, ±100mA trigger current	3/0 3/0 3/0	PASS 100mA. QBS to parent devices.
Early Life Fail Rate (ELFR)	JESD22-A108 JESD74 24hr/125C, Max Vdd, Max Duty Cycle.	120/0 510/0 870/0	PASS. QBS to parent devices.
High Temp Storage (HTS)	JESD22-A103D; 150C, 1000hrs	80/0 80/0 80/0	Lot1 @ 1000 PASS Lot2 @ 1000 PASS Lot3 @ 1000 PASS
Mechanical Qual Tests	JEDEC/MIL-STD-883	20/0	PASS

Notes:

1. For UHAST and Temperature Cycle, samples have been subjected to pre-conditioning per JESD22.
2. Please refer to product data sheet for ordering information.

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Document Revision History

Rev #	Description
1.0	Initial release – Qual Completion 2017/10/13

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